

FIG. 1

FIG. 2 is a block diagram of a DPTRCH frame structure. The frame is divided into five main sections: Pointer Field (22), Reserved Link Control (24), CRC (26), PCB (27), and Tail (28). A callout box 24 shows a detailed view of the Reserved Link Control field, which is further divided into Sequence Length (30) and HARQ (32).

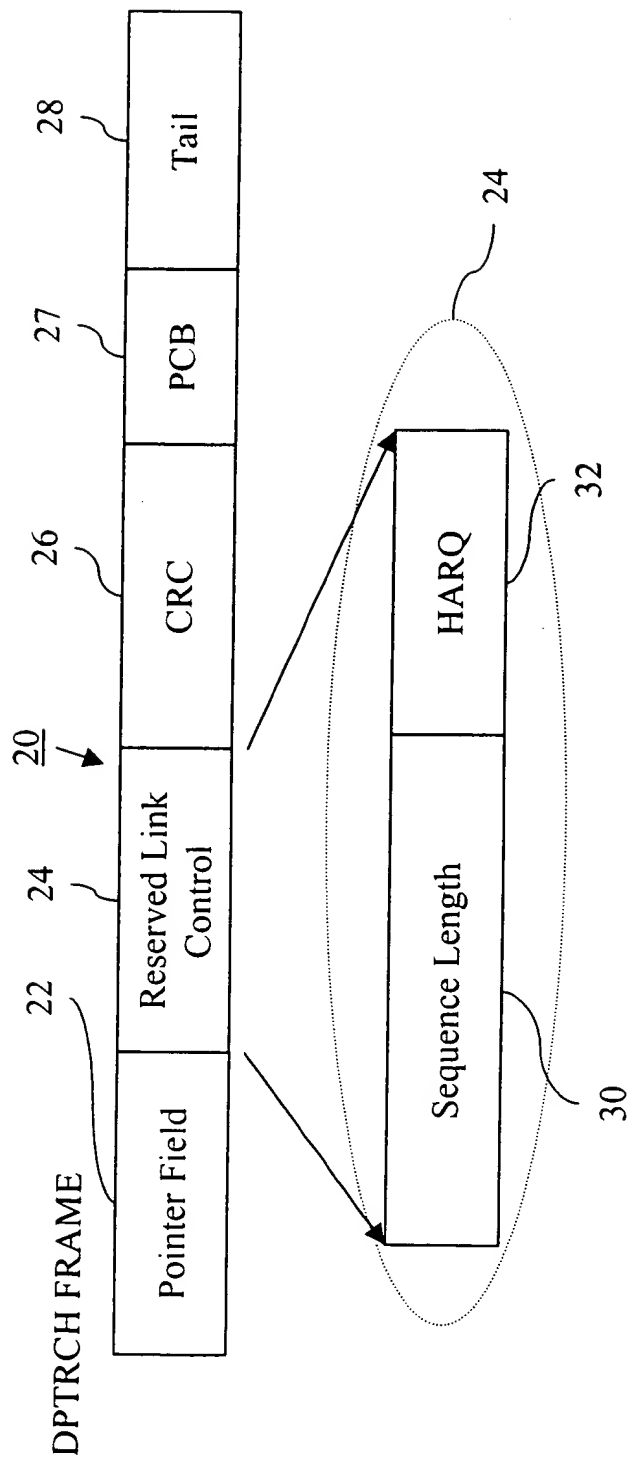


FIG. 2

NULL DPTRCH FRAME

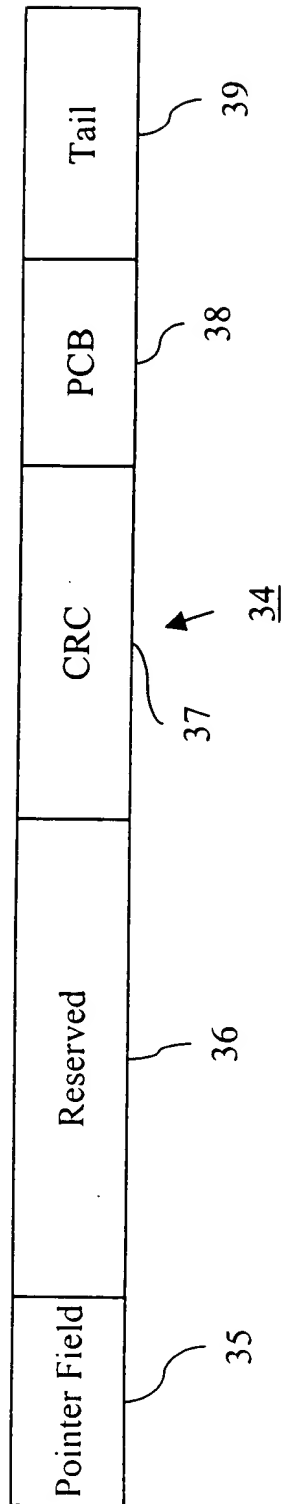


FIG. 3

SHCCH FRAME 42

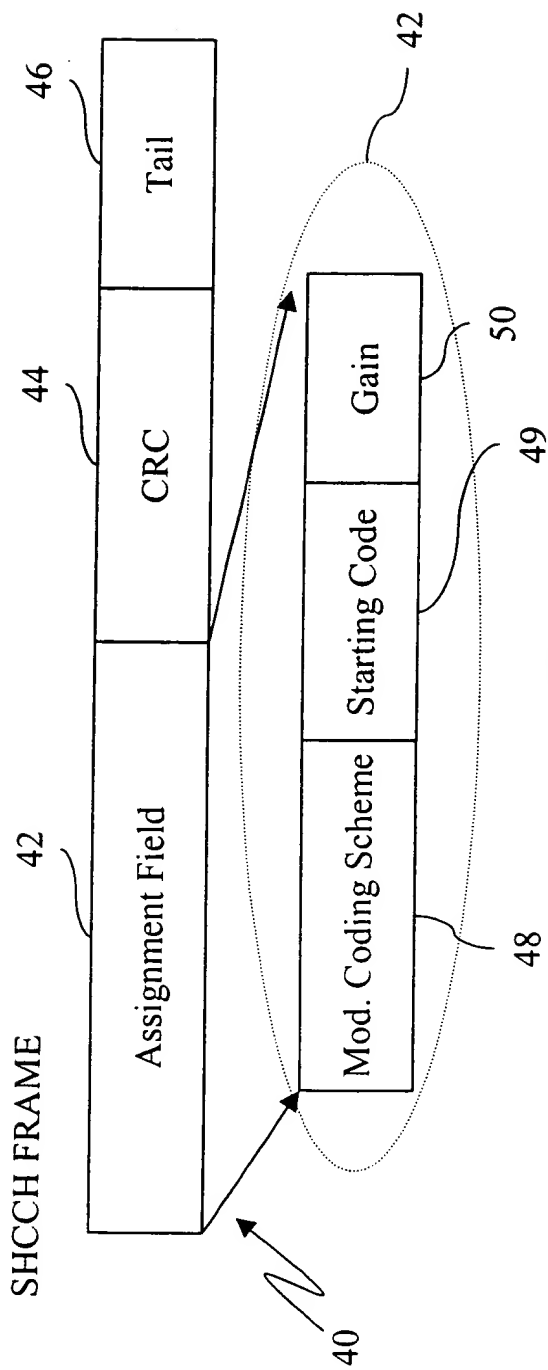
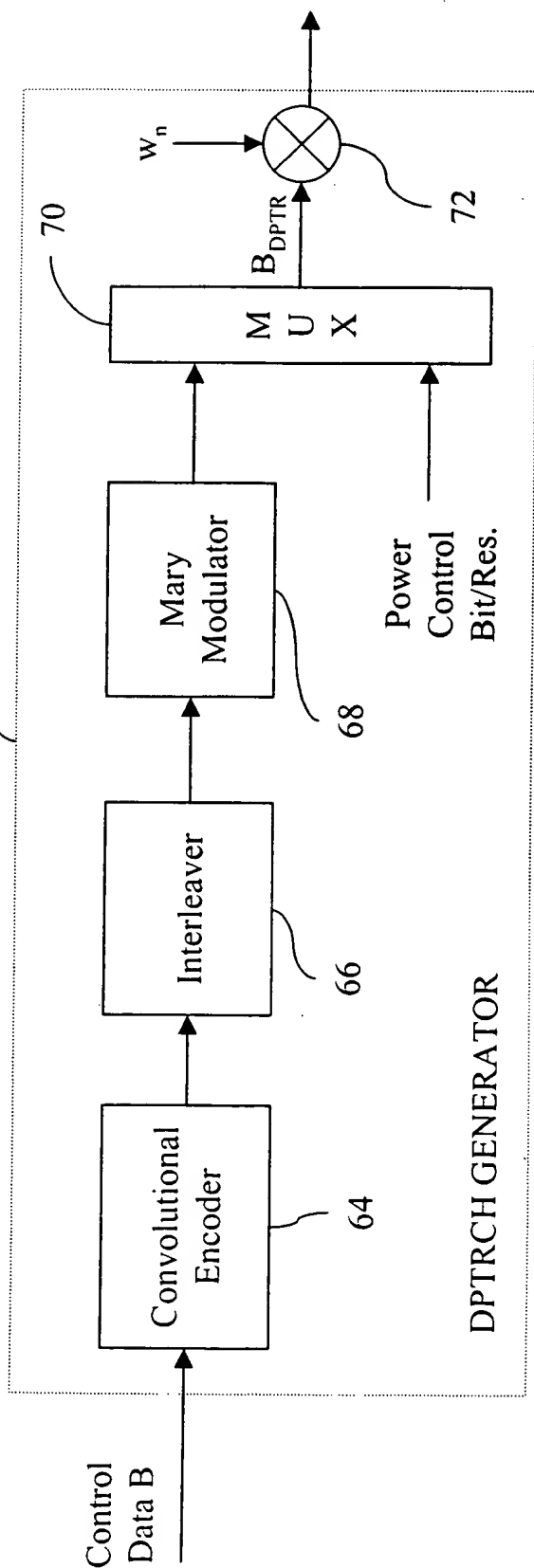


FIG. 4

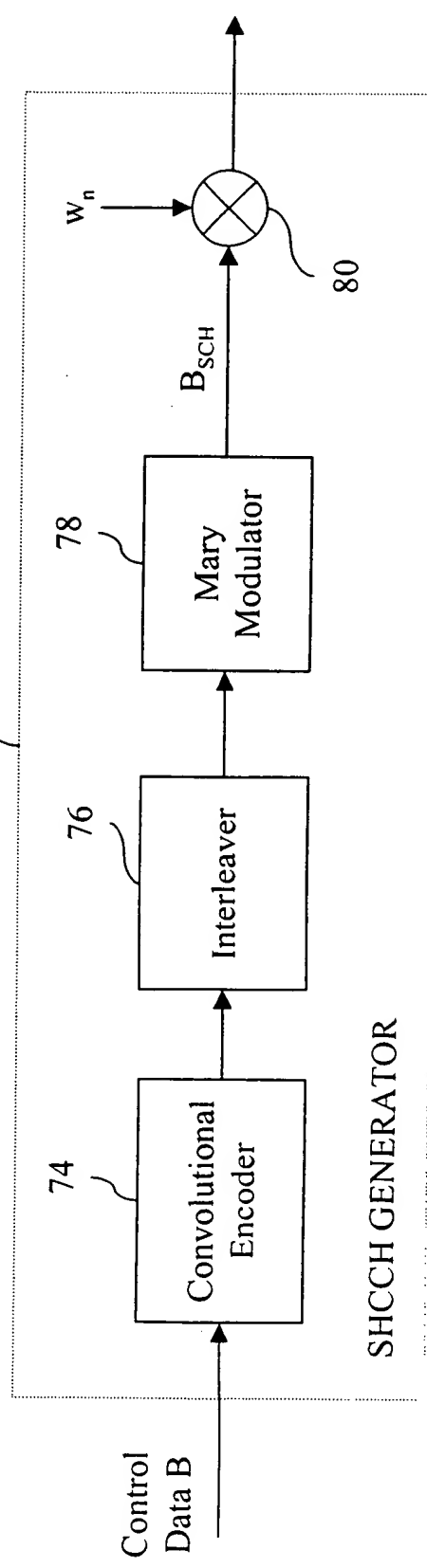
FIG. 5 is a block diagram of a system for generating a DPTRCH signal and an SHCCH signal. The system includes a DPTRCH GENERATOR (60) and an SHCCH GENERATOR (62). The DPTRCH GENERATOR (60) receives Control Data B and processes it through a Convolutional Encoder (64), an Interleaver (66), a Mary Modulator (68), and a MUX (70) to produce a DPTRCH signal (72). The SHCCH GENERATOR (62) receives Control Data B and processes it through a Convolutional Encoder (74), an Interleaver (76), a Mary Modulator (78), and a MUX (80) to produce an SHCCH signal (80). Both generators also receive Power Control Bit/Res. as input.

60



DPTRCH GENERATOR

62



SHCCH GENERATOR

FIG. 5